

cluster switches connected to the clusters to provide said mutually exclusive torus direction communication.--

--45. The array processor of claim 44 wherein each cluster includes an equal number of processing elements.--

--46. The array processor of claim 44 wherein at least one cluster includes a torus transpose pair of processing elements.--

--47. The array processor of claim 44 wherein the cluster switches provide inter-PE connectivity equivalent to a torus connected array.--

--48. The array processor of claim 44 wherein the cluster switches provide direct communication between processing elements in a transpose processing element pair within a cluster.--

--49. The array processor of claim 44 wherein the clusters of processing elements are scaleable.--

--50. The array processor of claim 44 wherein the processing elements of each cluster are located in close physical proximity to each other.--

--51. The array processor of claim 44 further comprising a single instruction multiple data (SIMD) controller which broadcasts data to said plurality of processing elements.--

--52. The array processor of claim 51 wherein each processing element performs a calculation and transmits the results of the calculation to a nearest neighbor processing element.--

--53. A method of forming clusters of processing elements comprising the steps of:
providing a torus array comprising a plurality of processing elements arranged in columns;

shifting the columns of the torus array vertically to form a rhombus;

wrapping the rhombus into a cylinder; and

taking horizontal slices of the cylinder to form clusters of processing elements.--

--54. An array processor, comprising:

processing elements (PEs) $PE_{i,j}$, where i and j refer to the respective row and column PE positions within a conventional torus-connected array, and where $i = 0, 1, 2, \dots, N-1$ and $j = 0, 1, 2, \dots, N-1$, said PEs arranged in clusters $PE_{((i+a) \bmod N), ((j+N-a) \bmod N)}$, for any i, j and for all $a \in \{0, 1, \dots, N-1\}$; and

cluster switches connected to said clusters providing inter-PE communications paths.--

--55. The array processor of claim 54, wherein said cluster switches are further connected to provide direct communications between PEs in a transpose PE pair within a cluster.--

--56. The array processor of claim 54, wherein said clusters are scaleable.--